LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A power estimation system, comprising:

a predetermined power characterization associated with at least one non-conventional circuit of a circuit design that relates power as a function of output drive load for a given non-conventional circuit, the predetermined power characterization is based on analyzing power consumption of the at least one non-conventional circuit for various associated output loads to determine a relationship of power as a function of output drive load; and

a power estimator computes power associated with the least one non-conventional circuit based on the predetermined characterization and a derived output drive load.

2. (Original) The system of claim 1, the at least one non-conventional circuit being a clock gater.

3. (Currently Amended) The system of claim 1, further comprising a plurality of pre-determined power characterizations associated with respective non-conventional circuit ~~type~~ types.

4. (Original) The system of claim 3, the respective predetermined power characterizations stored in a library, and the output drive load for each non-conventional circuit in the circuit design being derived employing a node capacitance list associated with a given circuit design instance.

5. (Original) The system of claim 3, the plurality of non-conventional circuit types being a plurality of clock gater types.

6. (Original) The system of claim 1, the output drive load for the at least one non-conventional circuit being derived employing node capacitance associated with a plurality of devices that are connected to an output of the at least one non-conventional circuit.

7. (Original) The system of claim 1, the power estimator computes power associated with at least one conventional circuit and adds the power associated with the at least one conventional circuit to the computed power associated with the least one non-conventional circuit to provide a total power estimate.

8. (Original) The system of claim 7, the power estimator computes power associated with the least one conventional circuit employing predetermined power characterizations that functionally relate switching power and leakage power to power related parameters.

9. (Original) The system of claim 8, the power related parameters comprising switching node capacitance and crossover current associated with switching power and leakage current associated with leakage power.

10. (Original) The system of claim 9, the switching power being computed employing a predetermined activity factor list and a node capacitance list associated with the at least one conventional circuit, the crossover power being computed employing predetermined crossover current equations and respective device gate widths, input voltage slopes and capacitive load parameters associated with a channel connected region associated with the at least one conventional circuit, and the leakage power being computed employing at least one predetermined leakage coefficient and the transistor gate area associated with the at least one conventional circuit.

11. (Currently Amended) The system of claim 1, the predetermined power characterization being determined by analyzing a spice characterization of the given non-conventional circuit to correlate power as a function of output drive load.

12. (Original) A system for estimating power for a circuit design, the system comprising:

a clock gater calculator that determines power consumed by at least one clock gater in a circuit design employing at least one predetermined characterization that correlates power as a function of output drive load for a given clock gater circuit; and

a power estimator that adds power associated with at least one conventional circuit of the circuit design to the power determined by the clock gater calculator to provide a total power associated with the at least one clock gater and the at least one conventional circuit.

13. (Original) The system of claim 12, the clock gater calculator determines power associated with a plurality of clock gater types by evaluating a corresponding functional relationship of power as a function of output drive load for each of the plurality of clock gater types.

14. (Original) The system of claim 12, the clock gater calculator derives an output drive load associated with a corresponding clock gater by parsing a node capacitance list associated with a circuit design instance.

15. (Original) The system of claim 12, the clock gater calculator determines power associated with a plurality of clock gaters by adding power determined for each of the respective clock gaters of the plurality of clock gaters.

16. (Original) A power estimation system, comprising:

means for determining power associated with non-conventional circuits in a circuit design based on a predetermined characterizations that relate power as a function of output drive

load for each of a given non-conventional circuit type, the predetermined power characterizations are predetermined based on analyzing power consumption for various associated output loads for each of a given non-conventional circuit type to determine a relationship of power as a function of output drive load for each non-conventional circuit type;

means for determining power associated with conventional circuits in the circuit design; and

means for computing total power of a circuit design based on the determination of power associated with non-conventional circuits and conventional circuits in the circuit design.

17. (Original) The system of claim 16, the non-conventional circuit types being clock gaters.

18. (Original) The system of claim 16, the means for determining power associated with non-conventional circuits further comprising means for deriving an output drive load associated with at least one non-conventional circuit.

19. (Currently Amended) A power estimation method for a circuit design, comprising:

computing power associated with at least one non-conventional circuit employing a predetermined characterization of power as a function of circuit design characteristics associated with the at least one non-conventional circuit;

computing at least one switching power related parameter associated with conventional circuits based on a first set of circuit design characteristics and a first predetermined characterization of switching power related parameters as a function of the first set of circuit design characteristics;

computing at least one leakage power parameter associated with conventional circuits based on a second set of circuit design characteristics and a predetermined characterization of leakage power related parameters as a function of the second set of circuit design characteristics;

computing power associated with conventional circuits employing the at least one switching power related parameter and the at least one leakage power related parameter; and

~~computing power associated with conventional circuits employing circuit design characteristics associated with conventional circuits; and~~

determining total circuit design power based on the computed power associated with non-conventional circuits and conventional circuits.

20. (Original) The method of claim 19, the non-conventional circuits comprising at least one clock gater device.

21. (Original) The method of claim 19, further computing power associated with a plurality of non-conventional circuit types based on a plurality of pre-determined characterizations for a plurality of non-conventional circuit types, such that each non-conventional circuit type is associated with a respective predetermined characterization.

22. (Original) The method of claim 19, the pre-determined characterizations for non-conventional being a pre-determined characterization of power as a function of output drive load.

23. (Cancelled)

24. (Original) The method of claim 19, further comprising:

executing an analysis tool for a plurality of circuit design instances;

computing a plurality of power estimates associated with the plurality of circuit design instances; and

comparing the power estimates to determine an optimal circuit design.

25. (Original) The method of claim 19, the non-conventional circuits being a circuit that employs drive fight.

26. (Original) A computer-readable medium having computer-executable instructions for performing the method of claim 19.

27. (New) The system of claim 1, the at least one non-conventional circuit being a circuit that employs drive fight.